REMARKS

Reconsideration of the present application is respectfully requested. Applicant has added claims to more clearly define what the Applicant regards as their invention. Support for the additions is found in the specification, the drawings, and in the claims as originally filed. Claims 12-17 are pending. Claims 23-36 have been added. No new matter has been added.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 12-17 under 35 USC 103(a) as unpatentable over Shin et al. (U.S. Patent No. 6,495,467) in view of Graas et al. (2002/008911) further in view of Lee et al. (US Patent No. 6,197,639). The Applicant respectfully traverses. The cited references, either individually or in combination, fail to anticipate or render obvious the Applicant's claimed invention. In particular, the cited references fail to teach or suggest the Applicant's required slot in the ILD which the applicant has taught and claimed to be a single structure requiring only one-dimensional lithography and enabling the bit line to contact a plurality of active areas.

The Examiner concedes in the Office Action of January 27, 2005 that Shin does not disclose the required slot in the interlayer dielectric. However, the Examiner states that Graas discloses the required slot pattern in the interlayer dielectric. The Applicant respectfully disagrees with the Examiner. It is Applicant's understanding that Graas lacks a "slot patterned in the ILD to *provide access to the active regions*" as Applicant has claimed in 12. In contrast, Graas only discloses a damascene structure where the interlevel dielectric

is patterned and etched to form a slot which does *not* provide access to active regions and instead requires the additional formation of individual vias (Graas, paragraph [0049]). Applicant's slot does not require vias because the slot *itself* provides access to the active regions. Similarly, Lee also fails to disclose the Applicant's claimed slot because Lee again describes *individual vias* contacting the individual active regions (Fig. 3, 43).

Therefore, all of the limitations of Applicant's independent claim 12 have not been taught or suggested by the cited references either alone or in combination and Applicant respectfully requests the removal of the 35 U.S.C. § 103 rejection.

New Claims

The new independent claims 23 and 30 both feature an etch stop layer forming the top surface of each gate stack, which is a feature not disclosed by any of the cited references. Noting new claims 24-29 and 31-37 depend upon 23 or 30, Applicant respectfully submits that new claims 23-37 are not anticipated or obvious in view of the cited references.

Applicant respectfully submits that in view of the arguments set forth herein, the applicable rejections have been overcome and the present application is in condition for allowance.